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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 February 2001 (22.02.2001)

PCT

(10) International Publication Number
WO 01/13436 A1

(51) International Patent Classification[7]: H01L 31/0328

(21) International Application Number: PCT/US00/20780

(22) International Filing Date: 16 August 2000 (16.08.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/148,702 16 August 1999 (16.08.1999) US

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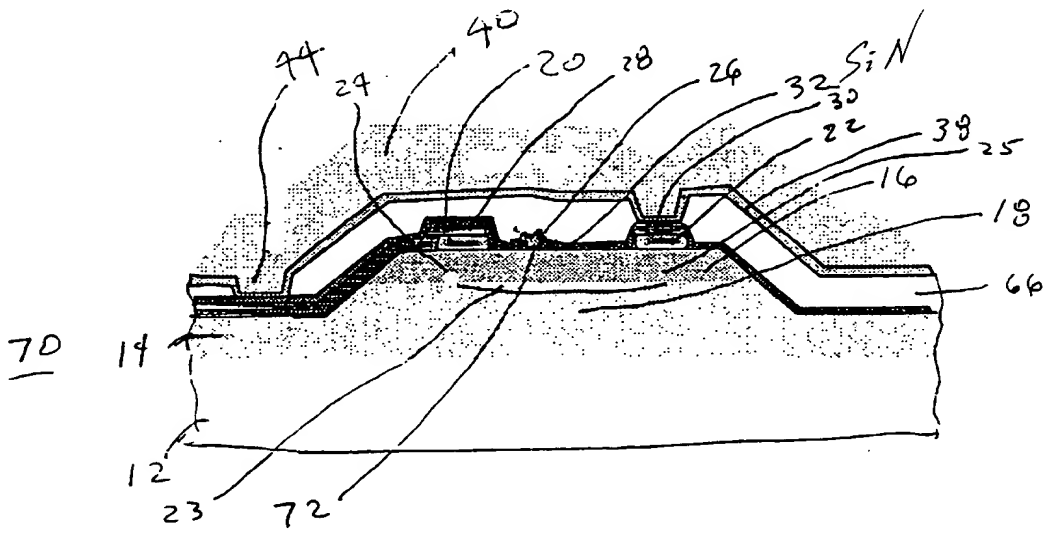
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PASSIVATION OF GAN BASED FETS



(57) Abstract: Surface passivation of GaN based FETs, including undoped AlGaN/GaN HEMTs and MISFETs, and doped GaN MESFETs, reduces or eliminates the surface effects responsible for limiting both the RF current and breakdown voltages of the devices. Passivation is provided through deposition of a layer (32) made of a dielectric, such as silicon nitride, silicon dioxide or polyimide, on a barrier layer (16) between a source (24) and a drain (25) of the FET (10).

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PASSIVATION OF GAN BASED FETS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates in general to GaN based field effect transistor (FET) devices, and methods for making the same, that employ passivation layers to improve device performance.

2. Description of the Background Art

There exists an ever-increasing need for high power, high efficiency microwave transistor amplifiers and switching devices in a variety of military and commercial wireless communications applications. This demand, coupled with advances in the growth of the group III nitrides, has spurred the development of high power GaN-based heterostructure field effect transistors (HFETs), including AlGaN/GaN high electron mobility transistors (HEMTs) and MISFETs (metal insulator semiconductor field effect transistors), and GaN MESFETs (metal semiconductor field effect transistors). However, a significant frequency-dependent slump or even collapse in drain current has plagued the saturated output power and efficiency realized by GaN based heterostructure FET technology. Efforts have been underway in several laboratories to understand this effect. However, to date, no solutions to the problem have been reported in the literature.

SUMMARY OF THE INVENTION

The present invention seeks to overcome the drawbacks of previous GaN based FET devices through provision of devices and methods for making the same that substantially reduce or eliminate the aforementioned frequency-dependent drain current slump. More particularly, the invention is directed to GaN based HFET devices that employ dielectric passivation layers on exposed AlGaN or GaN surfaces of the devices above the channel regions thereof. In experiments with AlGaN/GaN HEMTs and MISFETs, the use of a dielectric, e.g., Si_3N_4, passivation layer was found to control the undesirable frequency-dependent current and reduced breakdown voltage.

The inventors theorize that this frequency dependent current degradation is attributed to the presence of slow-acting trapping states between the gate and drain of the device. These trapping states are assumed to be associated with surface states created by dangling bonds, threading dislocations accessible at the surface, and ions absorbed from the ambient environment. These states trap electrons injected by the

gate and create a layer of charge at or near the surface that depletes the channel in the high field region between the gate and drain. Since the time constants of the trapping states in this surface layer range from seconds to microseconds, it is not possible for electrons contained in the surface layer to fully modulate the channel charge during large signal RF operation. The result is reduced RF current swing and output power. In addition, conduction and ionization along this surface layer limits the breakdown voltages of the devices.

Surface passivation is presumed to eliminate the surface dependent effects that produce the frequency-dependent current. In any event, experimental results establish that the use of the passivation layers substantially reduce or eliminate the frequency-dependent current slump and the related reduction of breakdown voltage. For example, in a first experiment, the addition of an Si_3N_4 passivation layer to undoped AlGaN/GaN HEMTs was found to increase the saturated power density by up to 100 % at 4 GHz and increased the breakdown voltage by an average value of 25 %. Furthermore, the passivation process achieved a state-of-the-art power density (4 W/mm at 4 GHz) for undoped AlGaN/GaN HEMTs on sapphire substrates. In comparison, to date, the state-of-the-art reported power performance for AlGaN/GaN HEMTs grown on SiC substrates is 9.1 W/mm at 8.2 GHz with the total power extracted from a single device of 9.8 W (8.2 GHz). In addition, state of the art power added efficiency (PAE) of 78% (1.8 W/mm) at 4 GHz was reported for a 1.5 mm periphery HEMT grown on a sapphire substrate.

In another experiment, a process for fabricating high-power MISFETs from undoped AlGaN/GaN heterostructures was developed where the devices are passivated post-growth with Si_3N_4. By adopting post-growth surface passivation, Class A microwave performance was obtained with maximum P_o's of 4.2 W/mm with 36% PAE at 4 GHz. Such performance for small devices on sapphire rival the present state-of-the-art results (4.6 W/mm with 44% PAE at 6 GHz) recently reported. These results also demonstrate the viability AlGaN/GaN MISFET devices has for high power microwave applications.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will be come apparent from the following detailed description of a number of preferred embodiments thereof, taken in conjunction with the accompanying drawings, in which:

FIGs. 1-9 are schematic illustrations of a number of fabrication steps that are employed to fabricate a GaN based FET in accordance with a preferred embodiment of the present invention, with FIG. 9 showing a complete FET having a passivation layer formed thereon in accordance with a first preferred embodiment of the present invention;

FIG. 10 is a schematic illustration of another passivated FET structure that is constructed in accordance with a second preferred embodiment of the present invention;

FIG. 11 is a schematic illustration of a third passivated FET structure that is constructed in accordance with a third preferred embodiment of the present invention;

FIG. 12 is a schematic illustration of a passivated MISFET structure that is constructed in accordance with a fourth preferred embodiment of the present invention;

FIG. 13 is a graph of output power and power-added efficiency (inset) as a function of drive for a $2 \times 125 \times 0.5\ \mu m^2$ HEMT before and after passivation at bias point of V_D=15 V, V_G=-4 V and frequency of 4 GHz (Z_L=131+j120, Z_S=22+j90 before passivation and Z_L=122+j51, Z_S=32+j85 after passivation);

FIG. 14 is a graph of breakdown voltage as a function of gate-drain spacing before and after device passivation for 0.5 μm gate length AlGaN/GaN HEMTs showing an increase in breakdown voltage of ~ 25 % with the addition of an Si_3N_4 passivation layer;

FIG. 15 is graph of output power and power-added efficiency as a function of drive for a passivated 2×0.4 μm AlGaN/GaN HEMT at a bias point of V_D=25 V, V_G=-4 V demonstrating 4 W/mm saturated output power (Z_L=187+j66, Z_S=106+j108); and

FIG. 16 is a graph of drain current as a function of applied gate bias voltage that compares these values for a MISFET constructed in accordance with the fourth preferred embodiment with those of an unpassivated HEMT.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to FIGs. 1-9, a fabrication process for forming a GaN based FET in accordance with a first preferred embodiment of the invention is illustrated. FIG. 9 illustrates a completed FET 10 that is either an AlGaN/GaN HEMT or a GaN MESFET, depending on the materials used in the various device layers to be

discussed presently. The FET 10 is formed on a substrate 12, that can be any suitable material, such as sapphire, SiC, GaN, etc. A buffer layer 14, preferably formed from GaN, and a barrier layer 16, which is made of undoped AlGaN in the case of an HEMT, and doped GaN in the case of a MESFET, are formed on the substrate 12. Together, these form a mesa 18 that serves to isolate the FET 10 from other FETs (not shown) on the substrate 12.

A source ohmic contact 20 and a drain ohmic contact 22 are disposed on top of the barrier layer 16 for making electrical connections to a source 24 and a drain 25, respectively, that are formed in the barrier layer 16. A channel region 23 is thus formed between the source 24 and the drain 25 near the top surface of the buffer layer 14 adjacent the interface between the buffer layer 14 and the barrier layer 16, as is conventional. A gate 26 is also disposed on the barrier layer 16 between the source and the drain contacts 20 and 22. First and second metal interconnects 28 and 30, which are preferably formed from gold, are disposed on the source and drain contacts 20 and 22, respectively.

The key to this and all embodiments of the invention is the provision of a dielectric passivation layer 32 that is disposed on top of the exposed surface of the barrier layer 16 between the source and drain contacts 20 and 22. Preferably, the passivation layer 32 is formed from silicon nitride, silicon dioxide, polyimide or any other suitable dielectric material. As will be discussed in greater detail herein in conjunction with the results of a number of experiments, the passivation layer 32 appears to reduce substantially, the charge trap phenomenon noted previously, thus increasing output power and breakdown voltage.

The completed FET 10 is illustrated in FIG. 9, which shows the addition of a resist layer 34 and an airbridge metallization 36 comprised of a priming metal layer 38 and a plated gold layer 40. The airbridge 36 provides a multi-level interconnect scheme as a well as a top plate 42 to a metal-insulator-metal (MIM) capacitor 44, a bottom plate 46 of which is formed by the first interconnect 28.

Fabrication of the FET 10 consists of seven mask levels, and these are illustrated sequentially in FIGs. 1-9. First, the buffer layer 14 and the barrier layer 16 are grown on the substrate 12 using an epitaxial growth process, such as organo-metallic vapor phase epitaxy, or molecular beam epitaxy (MBE). Next, as illustrated in FIG. 1, the definition of the active mesa 18 is performed using a first photo resist mask 50 and dry etching. Once the photo resist mask 50 has been patterned, the mesa 18 is etched using

either reactive-ion etching (RIE), electron-cyclotron resonance etching (ECR), or wet chemical etching, to etch the AlGaN/GaN barrier layer 16 and all or part of the GaN buffer layer 14.

In FIG. 2, the resist mask 50 used for etching the mesa 18 is removed and resist is applied and patterned to form a second resist mask 52 which defines a "lift-off" profile for definition of the ohmic contact metallization for the source and drain contacts 20 and 22. After resist patterning, a Ti/Al/Ti/Au metal stack multilayer 54 (shown as one layer) is deposited by evaporation or some other suitable means. After evaporation, solvents are used to dissolve the resist beneath the ohmic contact metal stack and hence lift off the overlaying metal in all areas other than where the multilayer 54 is deposited on the barrier layer 16. Following the removal of resist and excess metal, high temperature annealing (e.g., 800°C for 30 seconds) is used to diffuse the aluminum in the metal stack multilayer 54 into the AlGaN barrier layer 16 to form the ohmic source and drain contacts 20 and 22.

After the formation of ohmic contacts 20 and 22, another resist layer 56 is then deposited and patterned for formation of the gate 26 as shown in FIG. 3. The resist layer 56 is exposed and developed using either optical or electron beam lithography. After the patterning of the gate 26 in the resist layer 56, a Ni/Au metal stack 58 is deposited to form a rectifying contact to the AlGaN barrier layer 16. FIG. 3 shows a typical electron beam lithography process whereby the resist is exposed and developed to form the gate 26 in the shape of a "mushroom" whose large cross-sectional area minimizes the gate's electrical resistance. As in the case of the ohmic contact fabrication step, the excess metal is removed using the lift off technique as shown in FIG. 4, thereby leaving the gate 26 exposed between the source and drain ohmic contacts 20 and 22.

Deposition of the conductors for circuit connections and capacitor electrodes takes place after gate metallization as shown in FIG. 5. This step consists of patterning a photo resist layer 60, again using a lift off profile, depositing a metal layer 62, and then lifting off the excess metal using solvents. The deposited metal consists of a titanium adhesion layer and gold for low-resistance interconnects.

Following the deposition and patterning of the interconnect metal, the thin layer of dielectric 32 is deposited over the entire device wafer as shown in FIG. 6. Preferably, plasma-enhanced chemical vapor deposition (PECVD) is used for the silicon nitride deposition, although other deposition techniques can be used. However,

the refractive index of the silicon nitride must be close to 2.0 to assure high resistivity. Dielectric for integrated capacitors can also be deposited in this manner.

After deposition of the passivation layer 32, photoresist is deposited and patterned to form an etch mask 64 defining windows in the dielectric for electrical connections as illustrated in FIG. 7. Etching of the dielectric is accomplished using a CHF_3/O_2 plasma. After this etch step, the remaining resist is removed using solvents.

Formation of the airbridges 36 shown in FIG. 9 follows the deposition and patterning of the dielectric passivation layer 32. Referencing FIG. 8, this step consists of first, the deposition of the thin priming metal layer 38 on top of a layer of resist 66 patterned with holes where electrical contacts to the device are made. After the deposition of the priming metal layer 38, another level of resist is added to define the airbridges 36. Finally, the gold layer 40 is plated on top of the primer metal layer 38 to complete the airbridge spans 36 as shown in FIG. 9.

The preceding paragraphs sequence the steps of an entire AlGaN/GaN transistor/MMIC process employing a dielectric passivation layer placed after the gate level. Alternative schemes for passivating the surfaces of the devices are shown in FIGs. 10 and 11. The passivation scheme for the finished device shown in FIG. 10 entails depositing the silicon nitride passivation layer 32 on the surface of the AlGaN/GaN HEMT wafer prior to the mesa etch step and can even be deposited in the epitaxial reactor, in the case of $Al_XGa_{1-X}N$ with high X. In this case, windows are made in the dielectric at the gate, ohmic contact, interconnect, and airbridge via processing levels. MIM capacitors are formed using an additional dielectric layer processed in a manner identical to the process steps outlined above. Placing the dielectric passivation prior to other processing steps has the advantage of preventing contaminants to the silicon nitride/AlGaN interface. Control of these contaminants is critical to preventing the formation of conducting interface states between the Si_3N_4 and AlGaN. FIG. 11 shows a variant of the transistor embodiment of FIG. 10 whereby the dielectric layer 32 is placed on top of the device immediately after the mesa etching and windows are opened in the dielectric for the gates, ohmic contacts, and interconnect metallization.

In another experiment, a process was developed to fabricate MISFET devices from surface-passivated undoped AlGaN/GaN heterostructures on 2" diameter sapphire substrates via organometallic vapor phase epitaxy (OMVPE). These

structures which consist of a 34 nm $Al_{0.35}Ga_{0.65}N$ barrier on a 1.0 μm GaN buffer layer exhibited mobilities of around 1125 $cm^2/V \cdot s$ for 2DEG densities of $1.1 \cdot 10^{13}$ cm^{-2}. In this new process, both mesa isolation and ohmic window and metallization steps are done with photolithography whereas electron-beam lithography is used to define the gate with a 0.6 μm footprint. A Cl_2-based electron cyclotron resonance (ECR) dry-etch was used to define 150 nm mesas for device isolation. Patterned wafers were then passivated with a Si_3N_4 film 27 nm thick deposited in a commercial Si_3N_4 deposition system. From this point on, the heterostructure surface is hermetically sealed from subsequent processing steps. Ohmic windows were then patterned and etched through the dielectric in reactive ion etching (RIE) with CF_4. A Ti/Al/Ti/Au (20/100/50/150 nm) layered metallization was then evaporated and lifted off for ohmic contacts. Alloying of the layered metal was done in N_2 for 120-s at 850°C. From transfer-length method (TLM) structures, typical ohmic transfer resistances of around 1.2 ohms-mm with a sheet resistance of 530 ohms/sqr were measured. Prior to gate metallization with Ni/Au (20/400 nm), the dielectric under the gate was thinned down to roughly 18-nm by the same CF_4-based RIE used for the ohmic windows. The Schottky gate metallization was then evaporated and lifted off to define 0.6 μm gates.

The resulting structure is illustrated in FIG.12, which shows a MISFET 70 that includes all of the same elements as the HEMT 10 of FIG. 9. The only difference is that the gate 26 is formed on top of a thinned region 72 of the passivation layer 32.

To test the effectiveness of the passivation layer 32 in eliminating the charge traps, and thereby increasing the power density, the following experiments were conducted. First, DC, small signal and large signal characterization of a 2×125 ×0.5 μm^2 AlGaN/GaN HEMT, without passivation, was determined. In addition, breakdown voltage data on 2 × 75 × 0.5 μm^2 in-line gate finger devices with gate-drain spacings of 1.5 μm, 2 μm and 2.5 μm were taken. The maximum static current of the 2 ×125 ×0.5 μm^2 devices with 0 V on the gate (I_{DSS}) was found to be 520 mA/mm . The f_T and f_{max} were 25.3 GHz and 40.3 GHz respectively.

Loadpull data taken on the 2 × 125 × 0.50 μm^2 HEMT at 4 GHz using Focus Microwaves™ computer controlled microwave tuners showed the maximum saturated output power to be 0.5 W/mm at V_D= 10V and 1.0 W/mm at V_D= 15 V with associated maximum PAEs of 31 % and 36 % respectively. The gate-source bias for

both of these measurements was held constant at -4 V (120 mA/mm). The knee voltage, V_{knee}, was 4 V. A simple estimate of the maximum class A saturated output power based on the I-V characteristics of the device is given by

$$P_{sat} = \Delta I \Delta V / 8 \quad (1)$$

where $\Delta V = 2 (V_D - V_{knee})$ and $\Delta I = I_{D, max}$ (in mA/mm) and should be approximately 1.7 W/mm at V_D=15 V and 0.8 W/mm at V_D=10 V. Although this method of calculating the maximum power is approximate in nature, the disparity between the expected and measured output powers are too large to be ascribed to the calculation procedure or any small experimental errors (typical power measurement errors are ≤ 0.5 dB). It is assumed that the lack of available RF current limits the saturated power and efficiency.

The device wafers were then cleaned using acetone, methanol, isopropanol, and DI water (in this order) and then dipped in 30:1 buffered oxide etch for 30 seconds. No significant changes in device characteristics were seen after these cleaning and etch steps.

An IPE™ plasma-enhanced chemical vapor deposition (PECVD) system using Silane Si_3H_4 and ammonia (NH_3) sources was then used to deposit a 350 nm thick Si_3N_4 passivation layer on the device wafers at a baseplate temperature of 300 C. After the passivation, the DC, small signal, large signal and breakdown characteristics of the HEMTs were re-measured. The value of I_{DSS} (at low drain-source bias) of the 2 × 125 × 0.5 μm^2 device increased from 520 mA/mm to 640 mA/mm. Since the thermal conductivity of Si_3N_4 (0.37 W/cm-K) is approximately the same as that of sapphire (0.42 W/cm-K) and is very thin compared to the device dimensions (350 nm compared to microns), it is improbable that the passivation alters the thermal resistance of the device enough to increase the current. More likely, the rise in current is due to an increase in positive charge at the Si_3N_4/AlGaN interface, resulting in a higher sheet carrier concentration in the channel. Similar increases in sheet carrier concentration have been observed in other AlGaN/GaN surface passivation studies. A minor change in threshold voltage of the device from -4.5 V to -4.75 V after the passivation suggests that the maximum current is limited by the ungated regions of the device. Correspondingly, the small-signal transconductance increased

from 195 mS/mm to 210 mS/mm, consistent with the rise in current and small change in threshold voltage.

Small signal measurements also showed that the value of f_T decreased from 25 GHz to 22.7 GHz. The value of C_{gd} increased from 0.12 pF/mm to 0.17 pF/mm, which, in conjunction with the decrease in f_T, reduced f_{max} from 40.7 GHz to 34.0 GHz. The increase in C_{gd} is due, in part, to the increase in surface dielectric constant caused by the Si_3N_4 layer. In addition, the inability of the gate to charge the passivated surface layer confines the gate-drain depletion region to a smaller area near the gate edge, further increasing C_{gd}.

Unlike the small signal case, a tremendous difference in large signal performance before and after passivation was observed. FIG. 13 shows the difference in saturated power and PAE characteristics before and after passivation. As indicated, an increase in saturated output power of 100 % to 2.0 W/mm was measured at the same bias point and frequency which previously yielded only 1.0 W/mm. Using a simple loadline and accounting for the increase in maximum current, a value of 2.1 W/mm was expected. An increase in PAE from 36 % to 46 % was also noted as shown in the figure. The power sweep characteristics of the passivated device also show 1.5 dB lower small signal gain as expected because of the increased C_{gd} of the device. However in the case of the passivated device, the power saturation characteristics show less gain compression at higher drive which is consistent with the higher saturated output power achieved. The passivation appears to prevent steady-state depletion of the channel by the surface layer of extra trapped charge, and the gate can now completely modulate the channel. Hence, the full RF current swing of approximately 640 mA/mm is preserved.

Breakdown measurements were performed on 2 ×75 ×0.5 μm^2 devices with gate-drain spacings of 1.5 μm, 2.0 μm and 2.5 μm. The determination of the breakdown voltage was performed by pinching the channel off (V_{GS}= -8 V) and then raising V_{DS} until an appreciable amount of current (I_D=1 mA/mm) began to flow. The data shown in FIG. 14 demonstrate a 25 % average increase in drain-source breakdown voltage with a maximum of V_D=95 V for a 2.5 μm gate-drain spacing. Both before and after passivation, there was a sharp turn-on of drain current with a relatively unchanged gate current indicative of either surface conduction or avalanche breakdown. However, since the breakdown voltage increased after passivation, this

would suggest that prior to passivation the conduction and ionization of states in the surface layer dominates device breakdown while after passivation, avalanche breakdown near the gate edge dominates.

A second wafer was passivated using the same process. Again, the saturated power at 4 GHz was measured on a 2 × 125 ×0.5 μm device and an improvement from 1.67 W/mm (36 % PAE) at V_D = 15 V to 2.3 W/mm (41 % PAE) at the same bias point of V_D=15 V, V_G=-4 V (40 % improvement in power) was observed. As seen in FIG. 15, a 2 × 75 × 0.4 μm in-line finger device from this wafer yielded 4.0 W/mm (41 % PAE) of 4 GHz power at V_D=25 V, V_G=-4 V. This power density is the highest reported for undoped AlGaN/GaN HEMT structures with sapphire substrates.

Experiments were also conducted on MISFETs constructed in accordance with FIG. 12 to determine how their performance compared to conventional unpassivated HEMTs. The HEMTs had similar mobilities and 2DEG sheet density, and were also processed with a conventional 3-step HEMT process (mesa isolation, ohmic and gate metallizations). For these devices, the ohmic metallization was similar but thinner: Ti/Al/Ti/Au (20/100/50/50 nm). This resulted in transfer resistances of roughly 0.3 ohms-mm after a 30-s 800°C anneal in N_2. The remaining processing conditions used for these devices are similar to that used for the MISFETs when applicable.

Pulsed I-V characteristics were examined as a means to identify the DC-to-RF dispersion introduced in FETs from the interaction between channel electrons and the surface states. Such measurements have previously been applied to GaAs FETs to isolate the effects of relatively slow surface trapped charge on the microwave device performance. In this case, it was found that pulsing the gate voltage up from pinch off at a fixed drain bias result in a pronounced collapse of the I-V characteristics near the drain saturation voltage. In this case we have pulsed the gate of MISFETs and unpassivated HEMTs from pinch off to gate source voltages corresponding to full channel conditions at a fixed drain bias of 7 V. To avoid thermal effects, the gate is kept below pinch off and pulsed up, at a very low duty cycle, for 100 nsec once every 0.1 sec. The drain current is measured during the pulse and the resulting transfer characteristics are compared to those obtained with static conditions using a curve tracer. The results of these measurements are summarized in FIG. 16. The solid, open circle and square curves represent the static transfer characteristics of each device where the MISFET curve is shifted to the left (increase in V_p) from the

addition of the 18 nm Si_3N_4 layer under the gate metal. As shown for the MISFET, the pulsed drain current matches that of the static curve closely at all gate voltages above pinch off. This is in contrast to the unpassivated HEMT where the pulsed full channel current reaches only 40% of the static full channel value. These pulse drain currents represents the maximum current flowing during RF operation and as a result, higher microwave performance is expected and observed for the MISFETs.

Class A power sweeps at 4 GHz with 20, 25 and 28 V bias for the device of FIG. 1 exhibit maximum P_o from 2.8 W/mm to 4.2 W/mm with PAE of 35 - 37%. The P_o's measured here are within 10% of those predicted from the static I-V curves and suggest that these devices do not suffer from DC-to-RF dispersion, corroborating the results from the pulsed gate measurements. In contrast, unpassivated HEMTs do suffer from the DC-to-RF dispersion as the maximum P_o's are typically 25% lower than what is expected from their static I-V's at 15.0 V (1.5 W/mm measured as opposed to 2.1 W/mm expected). There was little increase in the maximum P_o's measured with increase bias. Measured gain curves exhibit some gain expansion before they start to compress. With bias, the output power at the 1-dB compression point increases from 2.3 W/mm at 20 V to 2.8 W/mm at 25 before dropping down to 2.2 W/mm at 28 V. The drop in the P_{1dB} point at 28 V may result from self-heating. Nevertheless, the power levels achieved with these MISFETs rival those reported elsewhere for small devices on sapphire substrates.

In conclusion, the experiments demonstrate that a Si_3N_4 passivation layer provides a means of reducing the surface layer mechanisms that limit the maximum RF current and breakdown voltage in AlGaN/GaN HEMT's. The experimental data presented show that the addition of a Si_3N_4 passivation layer to undoped AlGaN/GaN HEMT's increases the saturated power density by up to 100 % at 4 GHz and increases the breakdown voltage by an average value of 25 %. Furthermore, the passivation process achieved a state-of-the-art power density (4 W/mm at 4 GHz) for undoped AlGaN/GaN HEMTs on sapphire substrates. While it is presumed that the passivation eliminates the surface trapping effects that produce the frequency-dependent current, presumably by altering the properties of the surface states, a detailed description of the mechanism(s) responsible for the dispersion is admittedly lacking. Nevertheless, these promising initial results offer a simple means of reducing or eliminating large-signal slump in undoped AlGaN/GaN HEMTs and merit further study of the physical mechanisms responsible for the improvements.

Post-growth surface passivation has also allowed 100-μm GaN-based MISFETs on sapphire with an I_{dss} of 750 mS/mm, g_m of 105 mS/mm and f_T = 14 GHz to reach class A power levels at 4 GHz of up to 4.2 W/mm with 36% PAE. With no evidence for DC-to-RF dispersion, these results rival the present state-of-the art results of small AlGaN/GaN HFETs on sapphire previously reported. In addition, it is envisioned that adopting thinner AlGaN barrier will allow MISFETs to yield larger g_m's which result in higher f_T's and f_{max}. With higher power gains, larger P_o at higher frequencies is expected, especially on SiC substrates where the thermal conductivity is better and threading dislocation densities are lower.

Although the present invention has been disclosed in terms of a number of preferred embodiments, it will be understood that numerous modifications and variations could be made thereto without departing from the scope of the invention as set forth in the following claims. For example, the experimental results have established that surface passivation greatly improves the performance of GaN based HEMTs and MISFETs, however it is expected that similar performance improvements can be realized when surface passivation is employed with any type of GaN based FET.

CLAIMS

1. A GaN based field effect transistor (FET) device comprising:

a) a substrate;

b) a buffer layer disposed on said substrate;

c) a barrier layer disposed on said buffer layer, said barrier layer being formed from a material selected from the group comprising GaN and AlGaN, an interface between said barrier layer and said buffer layer defining a channel region in a top portion of said buffer layer;

d) a source and a drain disposed in said barrier layer; and

e) a dielectric passivation layer disposed on said barrier layer between said source and said drain.

2. The device of claim 1, wherein said passivation layer is formed from a dielectric material selected from the group comprising silicon nitride, silicon dioxide and polyimide.

3. The device of claim 1, wherein said substrate is formed from a material selected from the group comprising sapphire, SiC and GaN.

4. The device of claim 1, wherein said FET is a high electron mobility transistor, said barrier layer is formed from undoped AlGaN, and said device further comprises a gate disposed on said barrier layer between said source and said drain.

5. The device of claim 1, wherein said FET is a metal insulator semiconductor field effect transistor, said barrier layer is formed from undoped AlGaN, and said device further comprises a gate disposed on top of said passivation layer between said source and said drain.

6. The device of claim 1, wherein said FET is a metal semiconductor field effect transistor, and said barrier layer is formed from doped GaN.

FIG. 1

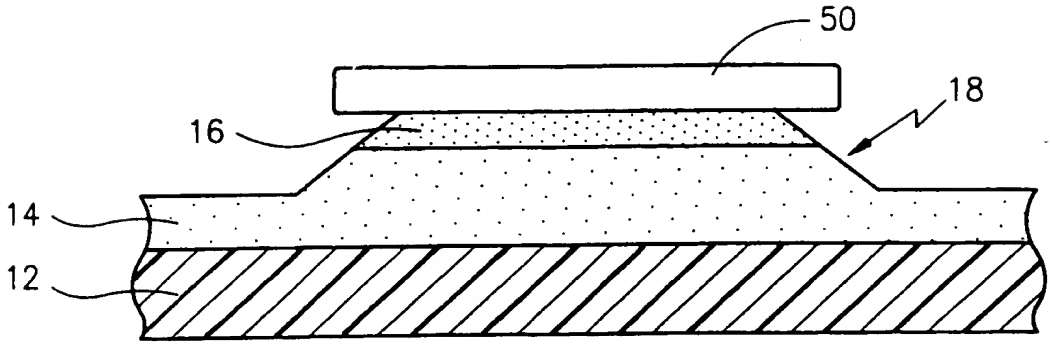


FIG. 2

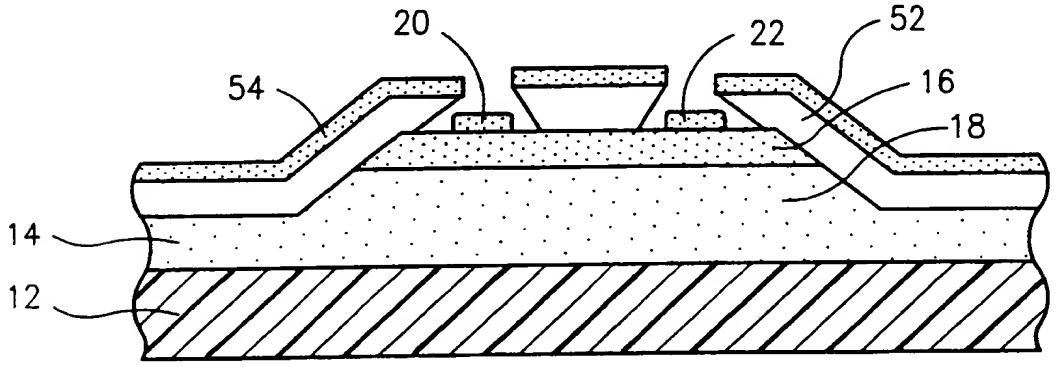


FIG. 3

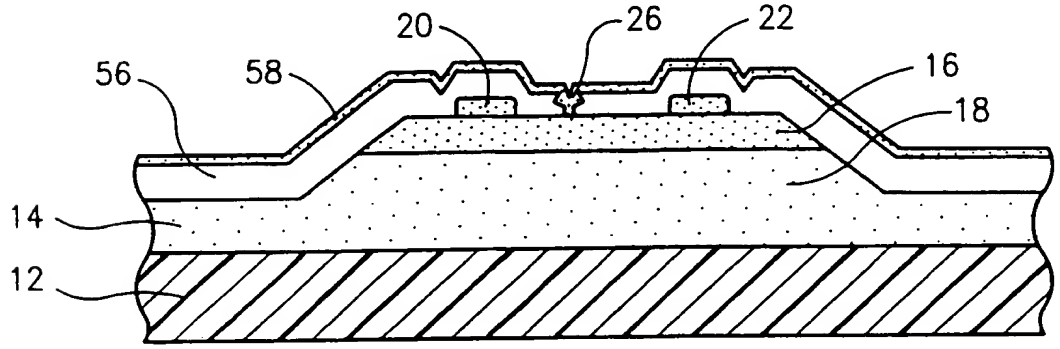


FIG. 4

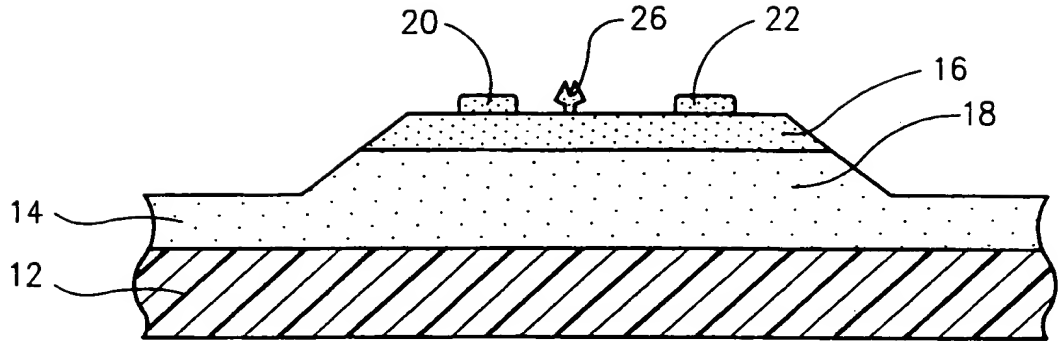


FIG. 5

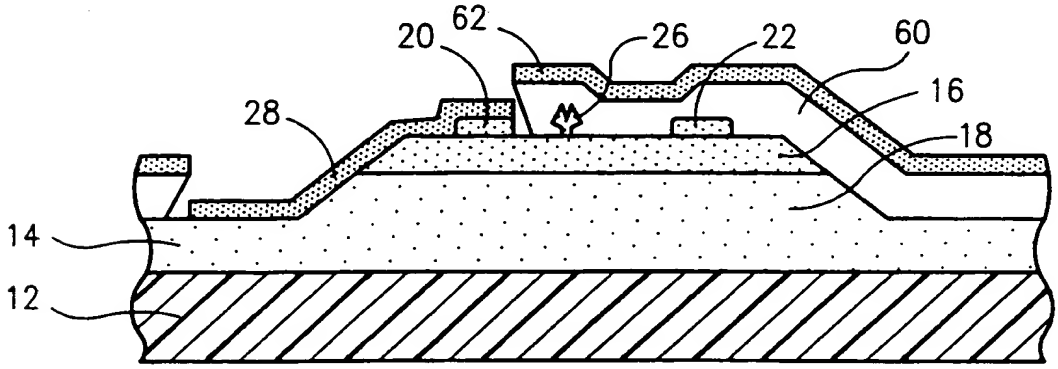


FIG. 6

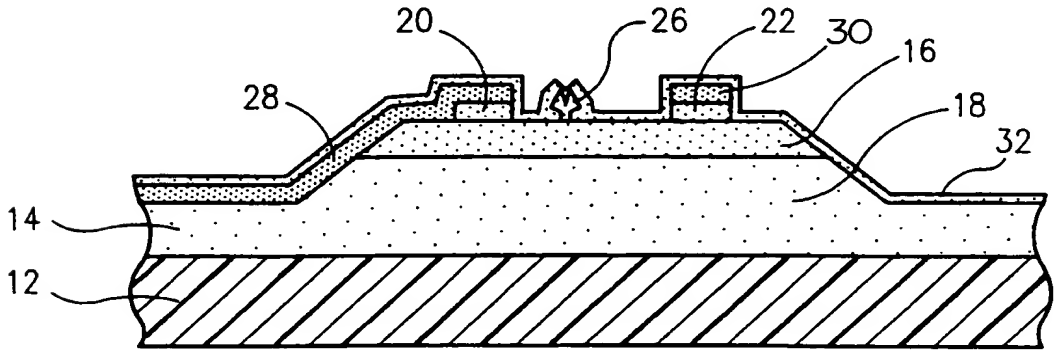


FIG. 7

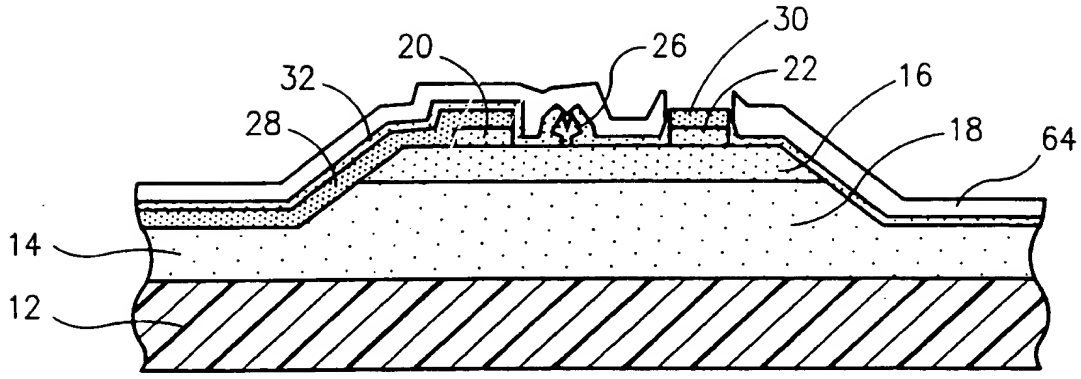
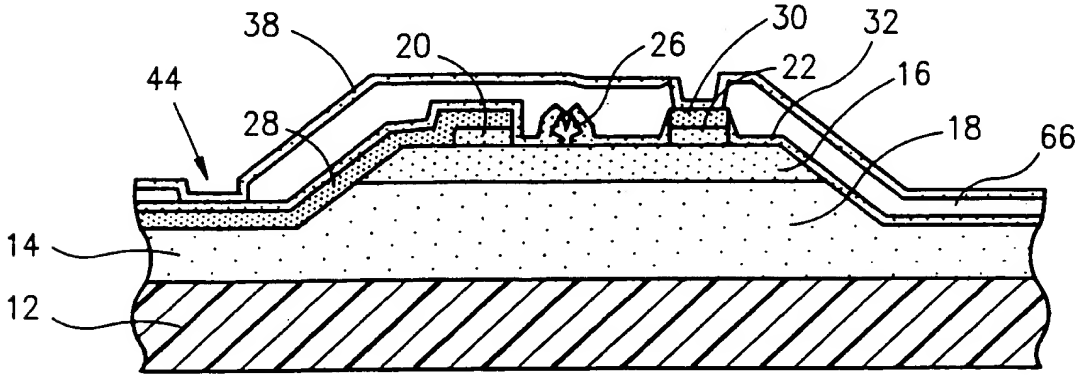


FIG. 8



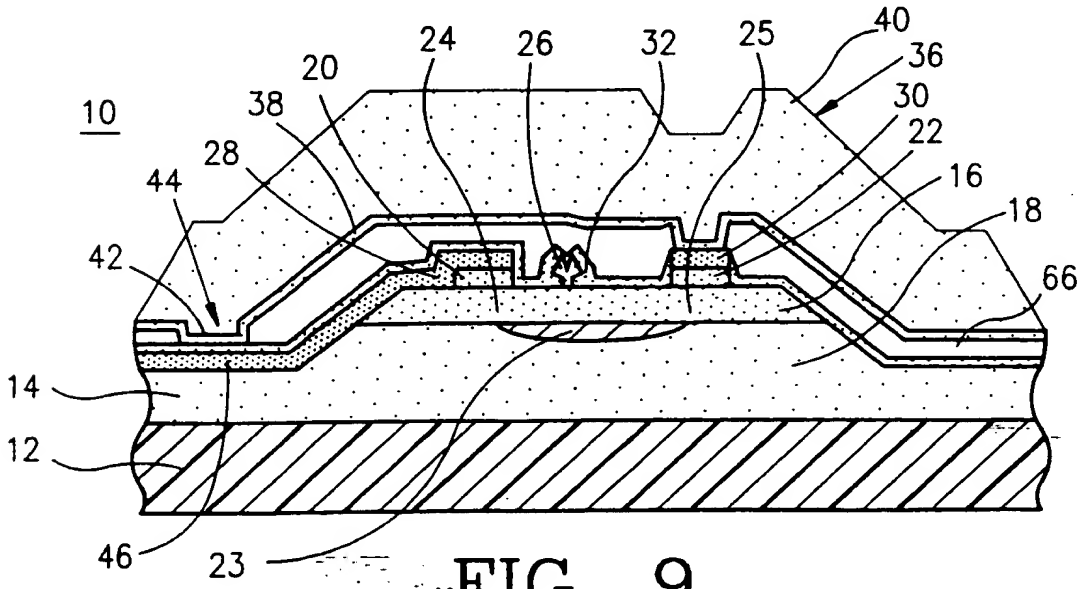


FIG. 9

FIG. 10

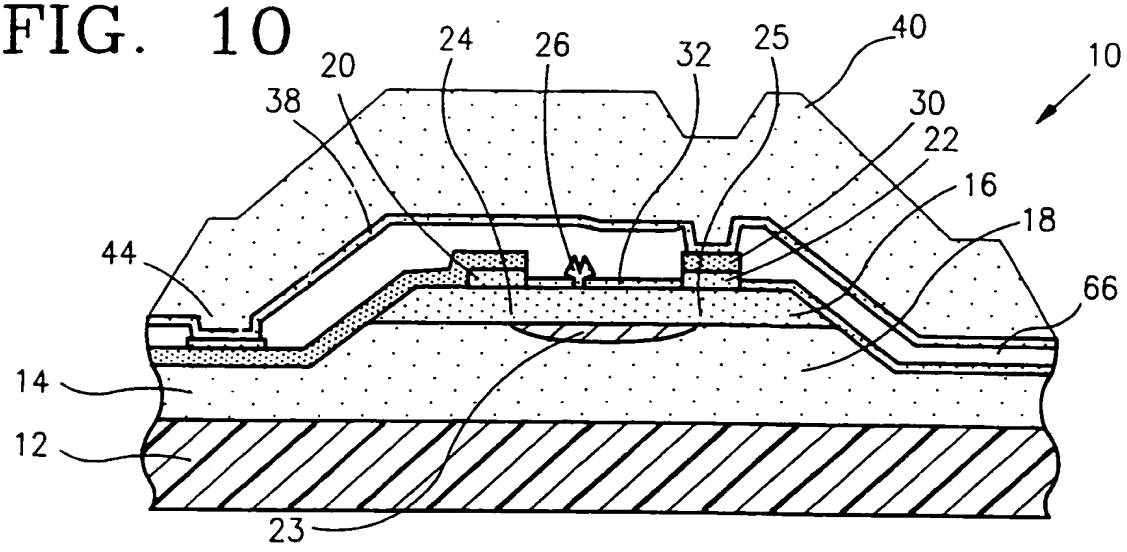


FIG. 11

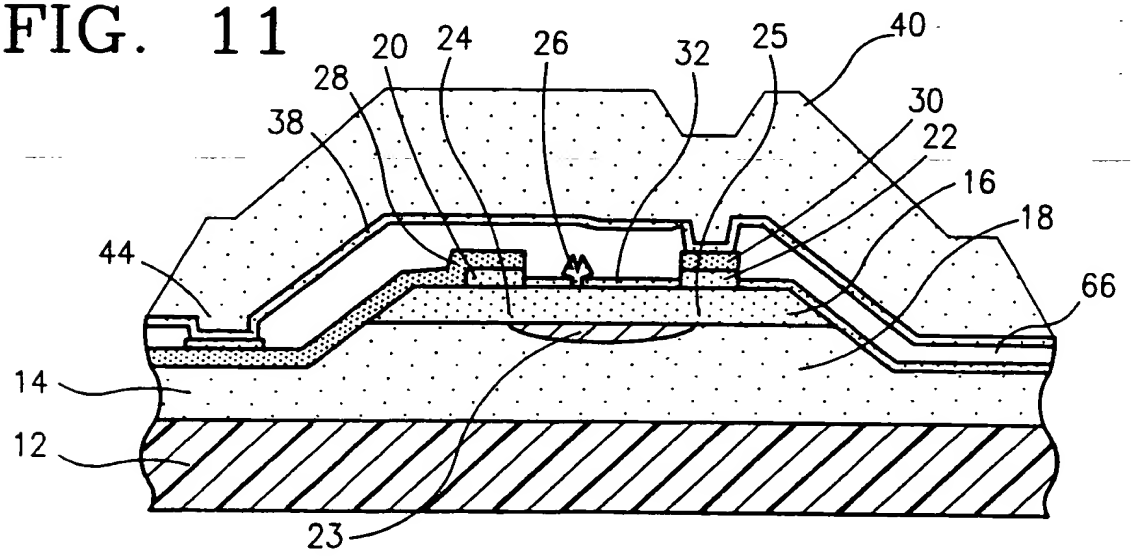


FIG. 12

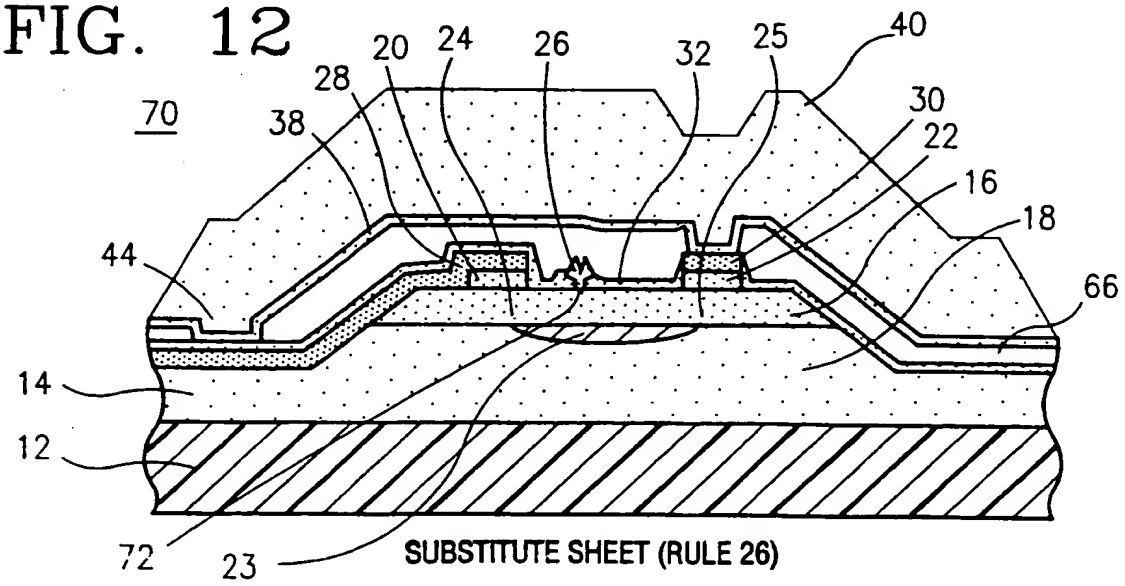


FIG. 13

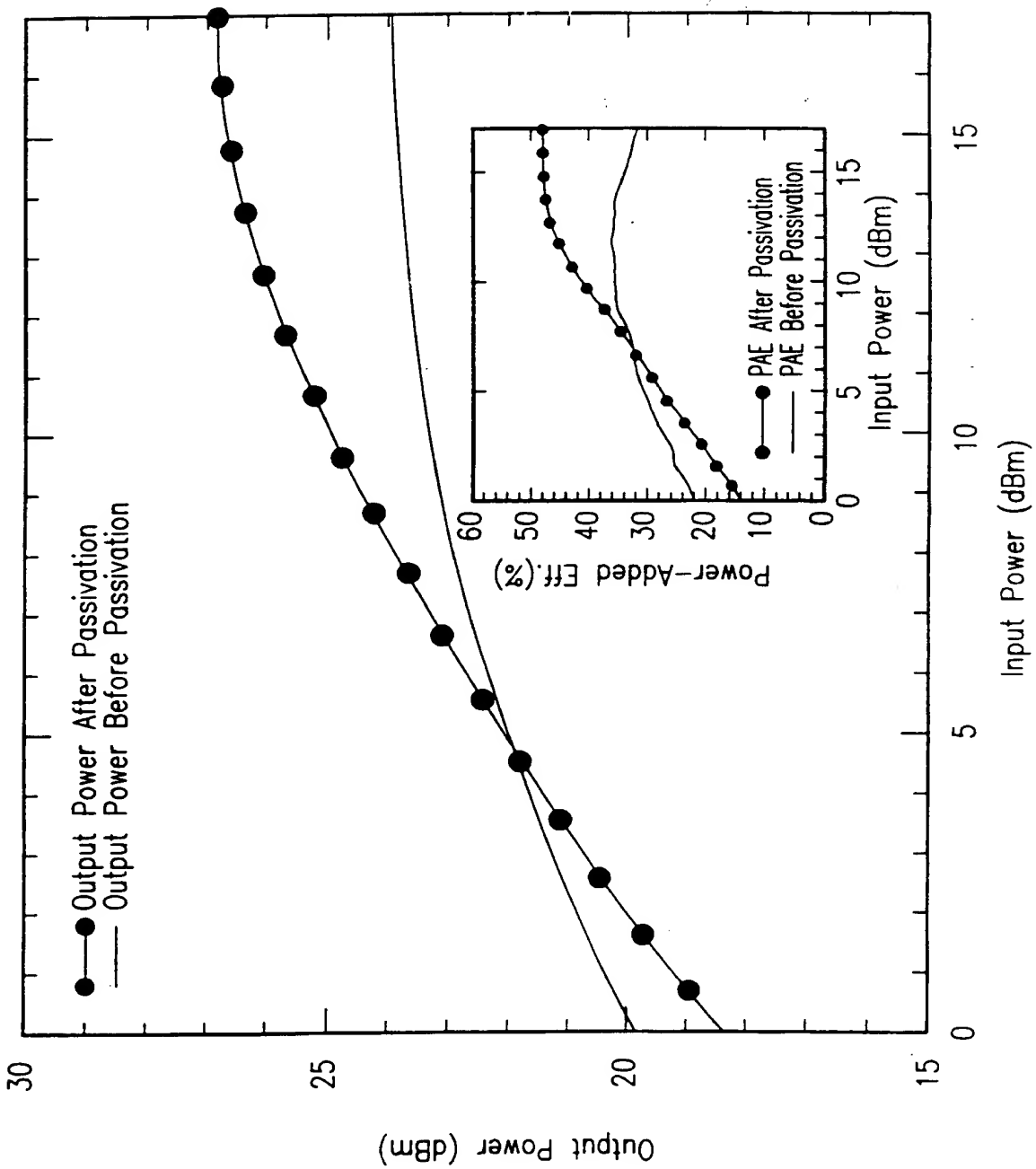


FIG. 14

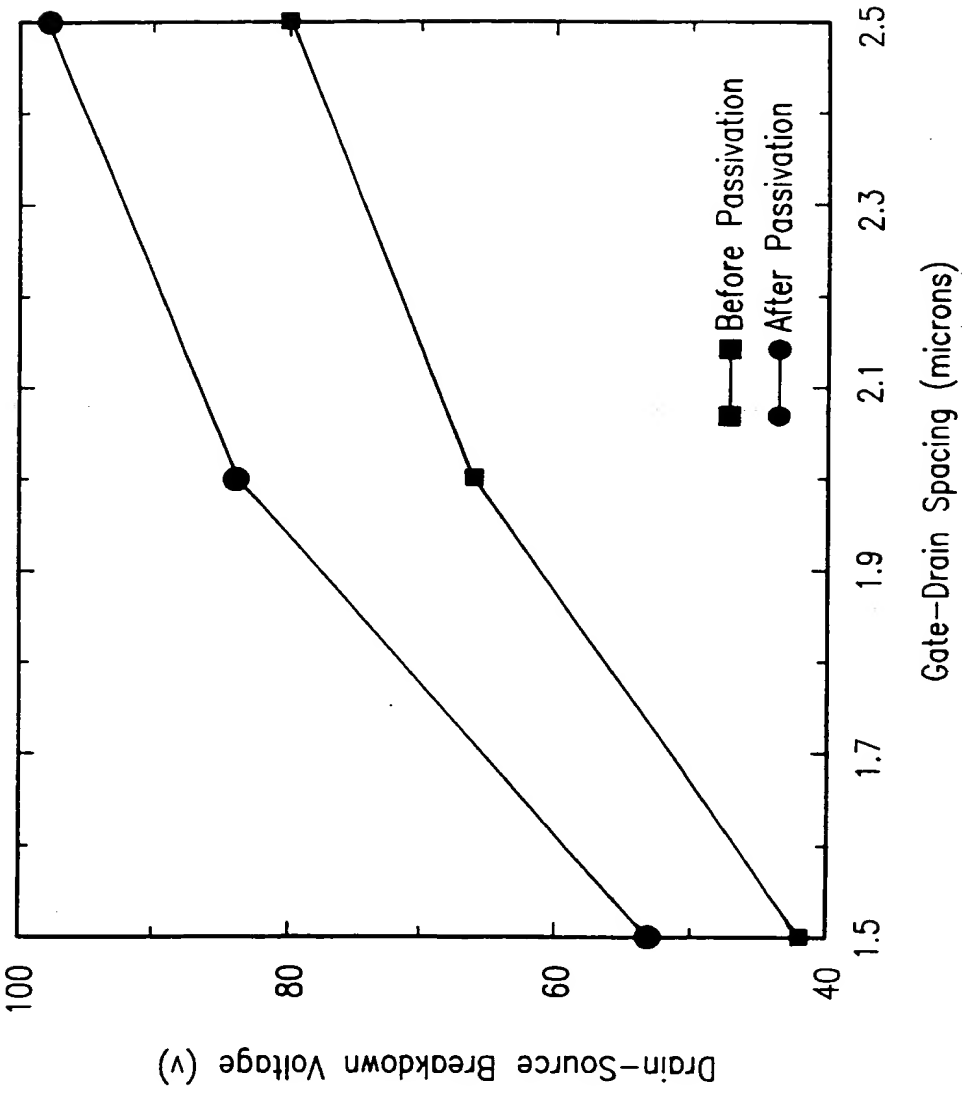

Drain–Source Breakdown Voltage (v)
100
80
60
40
1.5
1.7
1.9
2.1
2.3
2.5
Gate–Drain Spacing (microns)
Before Passivation
After Passivation

FIG. 15

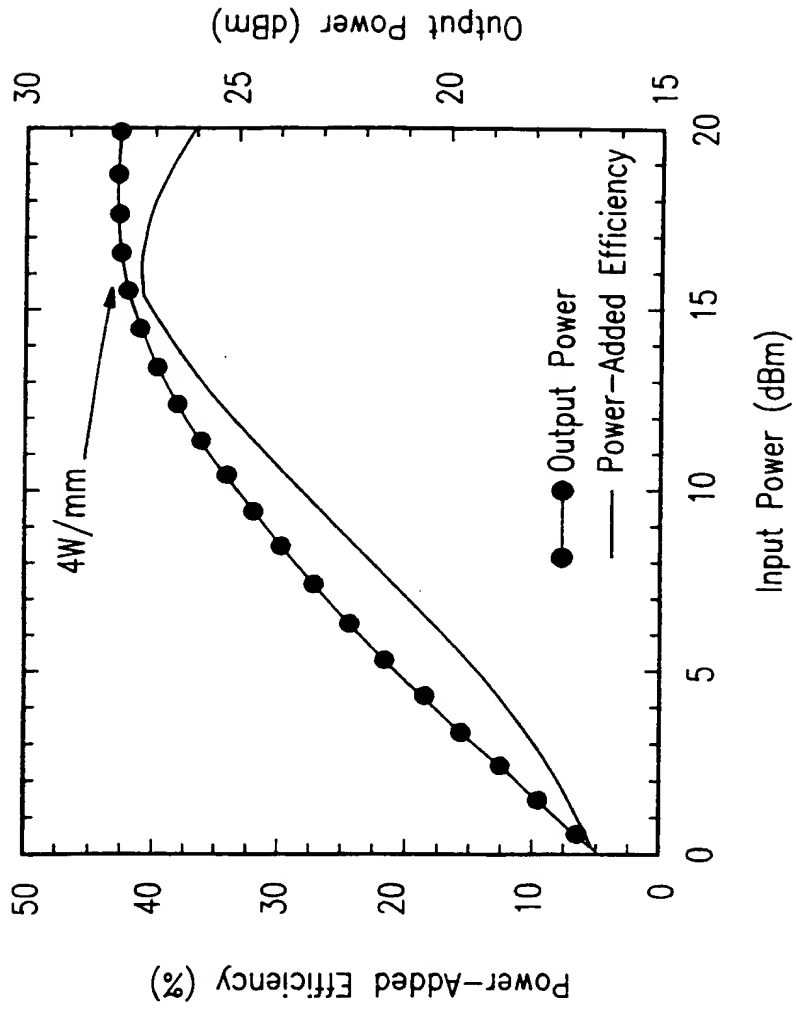
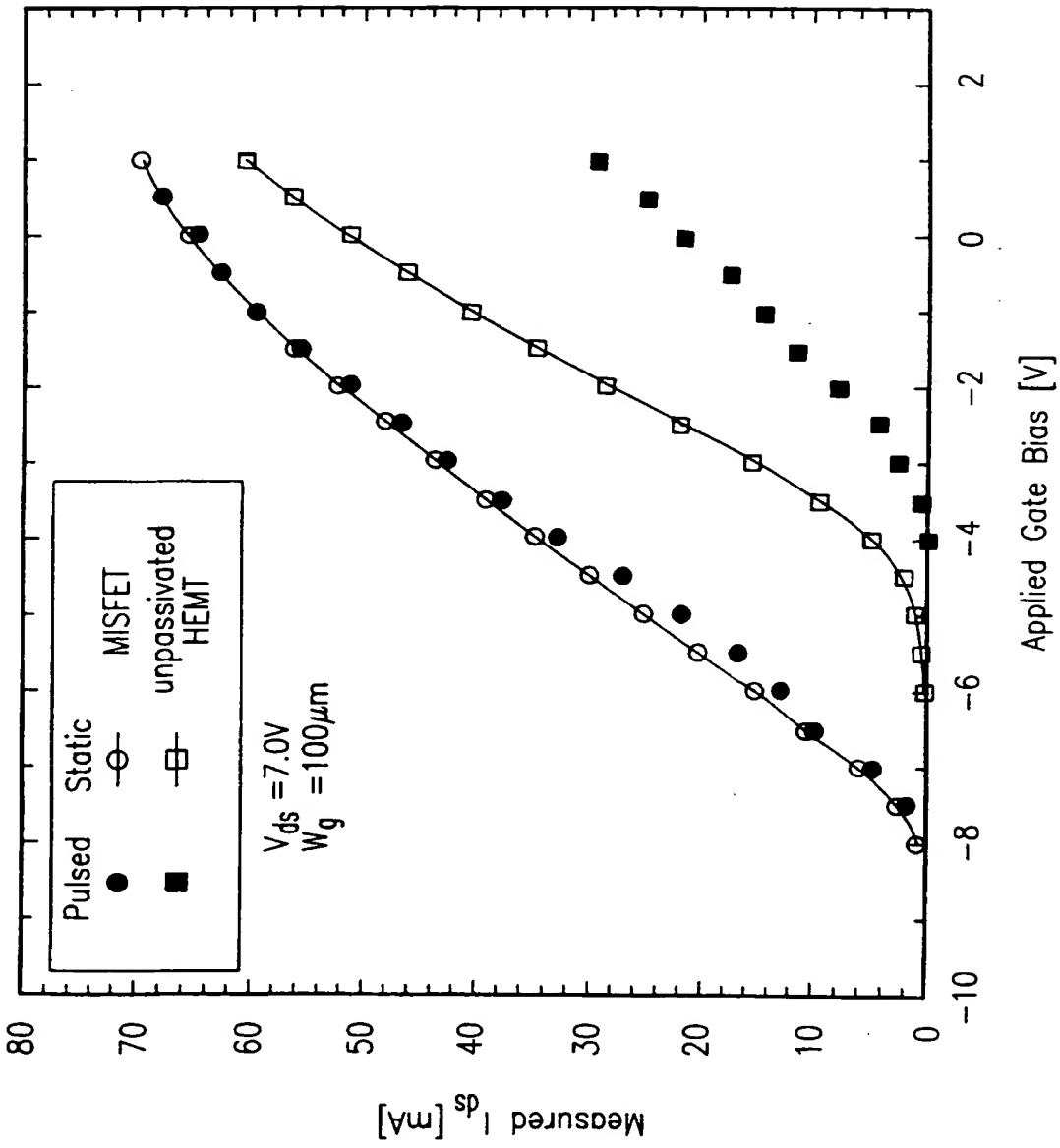


FIG. 16


Measured I_{ds} [mA]
80
70
60
50
40
30
20
10
0
−10
−8
−6
−4
−2
0
2
Applied Gate Bias [V]
Pulsed
Static
MISFET
unpassivated HEMT
V_{ds} =7.0V
W_g =100μm

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/20780

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 31/0328
US CL :257/192

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/192, 194, 613, 615

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,891,769 A (LIAW et al) 06 April 1999 (06.04.1999), see entire reference.	1-6
Y,P	US 6,100,549 (WEITZEL et al) 08 August 2000 (08.08.2000), see entire reference.	1-6
Y,P	US 5,990,531 (TASKAR et al) 23 November 1999 (23.11.1999), see entire reference.	1-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
05 OCTOBER 2000	08 NOV 2000

Name and mailing address of the ISA/US	Authorized officer
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Form PCT/ISA/210 (second sheet) (July 1998)*